

## CLAIMS

What is claimed is:

- 5 1. A method of performing a discrete cosine transform (DCT) using a microprocessor having an instruction set that includes SIMD floating point instructions, wherein the method comprises:
- receiving a block of integer data having C columns and R rows, wherein the block of integer data is indicative of a portion of an image; and
- for each row,
- 10 loading the row data into registers;
- converting the row data into floating point form, wherein the registers each hold two floating point row data values; and
- performing a plurality of weighted-rotation operations on the values in the registers, wherein the weighted-rotation operations are performed
- 15 using SIMD floating point instructions.
2. The method of claim 1, wherein said converting is accomplished using the pi2fw instruction.
3. The method of claim 1, wherein said weighted-rotation operations are accomplished using the pswap, pfmul, and pfpnacc instructions.
- 20 4. The method of claim 1, further comprising:
- for each row,

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altering the arrangement of values in the registers;

performing a second plurality of weighted-rotation operations on the  
values in the registers;

again altering the arrangement of the values in the registers;

5 performing a third plurality of weighted-rotation operations on the values  
in the registers;

yet again altering the arrangement of the values in the registers; and

performing a fourth plurality of weighted-rotation operations on the values  
in the registers to obtain intermediate floating point values.

10 5. The method of claim 4, further comprising:

for each row,

storing the intermediate floating point values to an intermediate buffer.

6. The method of claim 5, further comprising:

for two columns at a time,

15 loading data from two columns of intermediate data into each of a  
plurality of registers;

performing a plurality of weighted-rotation operations on the values in the  
registers, wherein the weighted-rotation operations for two  
columns are performed in parallel using SIMD floating point  
20 instructions.

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7. The method of claim 6, wherein said weighted-rotation operations for two columns at a time are accomplished using pfmul, pfsb, and pfadd instructions.

8. The method of claim 6, further comprising:

for two columns at a time,

5 as each weighted-rotation operation is done, storing weighted-rotation operation results to the intermediate buffer.

9. The method of claim 8, further comprising:

for two columns at a time,

10 retrieving weighted-rotation operation results from the intermediate buffer;  
performing a second plurality of weighted-rotation operations on the retrieved values;

again storing weighted-rotation operation results to the intermediate buffer as the weighted-rotation operations of the second plurality are done;

15 again retrieving weighted-rotation operation results from the intermediate buffer;

performing a third plurality of weighted-rotation operations on the retrieved values;

20 yet again storing weighted-rotation operation results to the intermediate buffer as the weighted-rotation operations of the third plurality are done;

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yet again retrieving weighted-rotation operation results from the intermediate buffer;

performing a fourth plurality of weighted-rotation operations on the retrieved values;

5 converting the weighted-rotation operation results from the fourth plurality to integer results.

10. The method of claim 9, further comprising:

for two columns at a time, writing the integer results to an output buffer.

11. A method of performing a discrete cosine transform (DCT) using a microprocessor  
10 having an instruction set that includes SIMD floating point instructions, wherein the method comprises:

receiving a block of integer data having C columns and R rows; and

for two columns at a time,

loading column data into registers;

15 converting the column data into floating point form, wherein the registers each hold a floating point column data value from two columns; and

performing a plurality of weighted-rotation operations on the values in the registers, wherein the weighted-rotation operations for two  
20 columns are performed in parallel using SIMD floating point instructions.

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12. The method of claim 11, wherein said weighted-rotation operations are accomplished using pfmul, pfsub, and pfadd instructions.

13. The method of claim 11, further comprising:

for two columns at a time,

5 as each weighted-rotation operation is done, storing weighted-rotation operation results to an intermediate buffer.

14. The method of claim 13, further comprising:

for two columns at a time,

10 retrieving weighted-rotation operation results from the intermediate buffer;  
performing a second plurality of weighted-rotation operations on the retrieved values;

again storing weighted-rotation operation results to the intermediate buffer as the weighted-rotation operations of the second plurality are done;

15 again retrieving weighted-rotation operation results from the intermediate buffer;

performing a third plurality of weighted-rotation operations on the retrieved values;

20 yet again storing weighted-rotation operation results to the intermediate buffer as the weighted-rotation operations of the third plurality are done;

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yet again retrieving weighted-rotation operation results from the intermediate buffer;

performing a fourth plurality of weighted-rotation operations on the retrieved values;

5 converting the weighted-rotation operation results from the fourth plurality to integer results.

15. The method of claim 14, further comprising:

for two columns at a time, writing the integer results to an output buffer.

10 16. A computer system comprising:

a processor having an instruction set that includes SIMD floating point instructions; and

a memory coupled to the processor, wherein the memory stores software instructions executable by the processor to implement the method of receiving a block of integer data having C columns and R rows, wherein the block of integer data is indicative of a portion of an image; and

for each row,

loading the row data into registers;

converting the row data into floating point form, wherein the registers each

20 hold two floating point row data values; and

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performing a plurality of weighted-rotation operations on the values in the registers, wherein the weighted-rotation operations are performed using SIMD floating point instructions.

- 5 17. A carrier medium comprising software instructions executable by a microprocessor having an instruction set that includes SIMD floating point instructions to implement a method of performing discrete cosine transform (DCT), wherein the method comprises:
- receiving a block of integer data having C columns and R rows, wherein the block of integer data is indicative of a portion of an image; and
- 10 for each row,
- loading the row data into registers;
- converting the row data into floating point form, wherein the registers each hold two floating point row data values; and
- performing a plurality of weighted-rotation operations on the values in the registers, wherein the weighted-rotation operations are performed
- 15 using SIMD floating point instructions.

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